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10/824,594	04/15/2004	Fumitoshi Mizutani	ND-448US	6639

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EXAMINER	
TRUONG, LOAN	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,594	MITZUTANI ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 20-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's argument filed July 02, 2007 in application 10/824,594.

2. Claims 1-9 and 20-24 are presented for examination, claim 8 had been amended, claims 20-24 are newly added and claim 10-19 are cancelled.

Response to Arguments

3. Applicant's arguments filed have been fully considered but they are not persuasive.

In regard to claim 1, applicant stated that Iselt fails to disclose a first and second processing means and adjusting orders of output data from said first and second information processing means. Given the broadest interpretation of the claim language, the examiner equates the two data streams of Iselt to applicant's two processing means. The term an information apparatus, comprising: first and second information means is broad enough to encompass the synchronizing data streams of Iselt where the different paths in which the data travel would subject them to different process thereby creating different processing means. Also, refering to Iselt fig. 3b, the buffer is deleted thus shifted to adjust the first and second processing means so as to correspond to each other. Applicant mentions that the Iselt orders of the output data are unaffected. Deleting a first entry in the buffer would change the order of data in the buffer thereby changing the orders of the data. Furthermore, the claim language provided no specific ways to adjust the two processing means to correspond to each other.

Claims 2-4 contain the same limitations as claim 1 and therefore the rejection are maintained.

In regard to claim 5, applicant stated that Iselt fails to disclose first and second information processing means and adjustment means including re-construction means for re-constructing a plurality of data of said second information processing means. Similar to claim 1, examiner equates applicant's two processing means to Iselt two data stream and when comparing detect various discrepancies in the data streams, faulty ATM cells may be removed from the data stream to reconstructing a data of said second information processing means.

Claims 6-7 are dependent on a rejected claim and contains similar limitations and therefore are rejected.

Claims 8 and 9 inherits all features and limitations thereof and therefore remains rejected based on reasons stated above.

In regard to claim 4, applicant stated that since Iselt already provides data monitoring and error correction there is no reason to combine Zhang. Examiner would like to point out that Zhang is combined with Iselt to teach the limitations of designating a frequency to be performed to a lower than a frequency with which the output data of said first and second information means. Zhang focus on adjusting means for adjusting the frequency of data output similar to applicant reasons for doing the same and thus provide a significant need to combine Zhang and Iselt to provide an adjusting means to adjust the frequency of output data.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3, 5-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Iselt (US 6,917,582).

In regard to claim 1, Iselt disclosed an information processing apparatus, comprising:

first and second information processing means for performing the same process in synchronism with each other (*ATM cell stream is split into two redundant data streams that are routed via different paths, fig. 1, col. 3 lines 5-10)*; and

adjustment means (*merge the data streams, fig. 1, col. 3 lines 5-20)* for adjusting orders of output data from said first and second information processing means so as to correspond to each other to discriminate whether or not the output data coincide with each other (*fig. 3b-3c, comparison of the two ATM cells leads to an inequality in the pair-by-pair comparison during failure recognition phase, col. 4 lines 43-57 and col. 5 lines 1-16).*

In regard to claim 2, Iselt disclosed an information processing apparatus as claimed in claim 1, wherein said adjustment means includes first storage means for storing the output data of said first information processing means and second storage means for storing the output data of said second information processing means (*Buffer memories P0 and P1 in which ATM cells are written to, fig. 1, P0, P1, col. 5-16).*

In regard to claim 3, Iselt disclosed an information processing apparatus as claimed in claim 2, wherein said adjustment means compares when the amount of output data stored in any one of said first and second storage means reaches a predetermined amount (*ATM cells are always compared over a length of k ATM cells, col. 3 lines 50-55)*, the output data of said first information processing means stored in said first storage means and the output data of said second information processing means stored in said second storage means with each other (*Buffer memories P0 and P1 in which ATM cells are written to, fig. 1, P0, P1, col. 5-16)* with the output data adjusted in order so as to correspond to each other to discriminate whether or not the output data coincide with each other (*fig. 3b-3c, comparison of the two ATM cells leads to an inequality in the pair-by-pair comparison during failure recognition phase, col. 4 lines 43-57 and col. 5 lines 1-16).*

In regard to claim 5, Iselt disclosed an information processing apparatus, comprising:

first and second information processing means for performing the same process in synchronism with each other (*ATM cell stream is split into two redundant data streams that are routed via different paths, fig. 1, col. 3 lines 5-10)*; and

adjustment means including re-construction means for re-constructing a plurality of output data of said second information processing means based on a plurality of output data of said first information processing means (*merge the data streams, fig. 1, col. 3 lines 5-20)*; and

comparison means for comparing the output data of said first information processing means and the output data of said second information processing means re-constructed by said re-construction means with each other (*fig. 3b-3c, comparison of the two ATM cells leads to an*

inequality in the pair-by-pair comparison during failure recognition phase, col. 4 lines 43-57 and col. 5 lines 1-16).

In regard to claim 6, Iselt disclosed an information processing apparatus as claimed in claim 5, wherein said adjustment means includes first storage means for storing the output data of said first information processing means and second storage means for storing the output data of said second information processing means (*Buffer memories P0 and P1 in which ATM cells are written to, fig. 1, P0, P1, col. 5-16)*, and said re-construction means (*merge the data streams, fig. 1, col. 3 lines 5-20)* changes the order of the output data of said second information processing means stored in said second storage means based on the order of the output data of said first information processing means stored in said first storage means (*assuming that the trailing data stream D0 has been lost, the leading data stream D1 becomes the merged output, fig. 3b, comparison of the two ATM cells leads to an inequality in the pair-by-pair comparison during failure recognition phase, col. 4 lines 43-57 and col. 5 lines 1-16).*

In regard to claim 7, Iselt disclosed an information processing apparatus as claimed in claim 5, wherein said adjustment means includes first storage means for storing the output data of said first information processing means and second storage means for storing the output data of said second information processing means (*Buffer memories P0 and P1 in which ATM cells are written to, fig. 1, P0, P1, col. 5-16)*, and said re-construction means (*merge the data streams, fig. 1, col. 3 lines 5-20)* divides and re-couples the output data of said second information processing means stored in said second storage means based on the output data of said first

information processing means stored in said first storage means (*replacing the faulty/missing ATM cell with a corresponding ATM cell taken from an intact, other redundant sub-system, col. 2 lines 52-61).*

In regard to claim 8, Iselt disclosed an information processing apparatus, comprising:

first and second information processing means for performing the same process in synchronism with each other (*ATM cell stream is split into two redundant data streams that are routed via different paths, fig. 1, col. 3 lines 5-10)*; and

adjustment means (*merge the data streams, fig. 1, col. 3 lines 5-20)* for selecting one of data of a second output of said second information processing means which corresponds to one of data of a first output of said first information processing means to detect whether or not the data of the first and second outputs coincide with each other (*fig. 3a-3c, comparison of the two ATM cells leads to an inequality in the pair-by-pair comparison during failure recognition phase, col. 4 lines 43-57 and col. 5 lines 1-16).*

In regard to claim 9, Iselt disclosed an information processing apparatus as claimed in claim 8, wherein said adjustment means (*merge the data streams, fig. 1, col. 3 lines 5-20)* includes first storage means for storing the data of the first output of said first information processing means and second storage means for storing the data of the second output of said second information processing means (*Buffer memories P0 and P1 in which ATM cells are written to, fig. 1, P0, P1, col. 5-16)*, and said adjustment means (*merge the data streams, fig. 1, col. 3 lines 5-20)* searches said second storage means for one of the data of the second output

corresponding to one of the data of the first output of said first information processing means stored in said first storage means (*fig. 3a-3c, comparison of the two ATM cells leads to an inequality in the pair-by-pair comparison during failure recognition phase, col. 4 lines 43-57 and col. 5 lines 1-16).*

In regard to claim 20, Iselt disclosed the information processing apparatus according to claim 1, wherein said adjustment means comprises error control means controlling an output of said adjustment means such that one of said output data of said first and second information processing means is outputted from said adjustment means (*Buffer memories P0 and P1 in which ATM cells are written to, fig. 1, P0, P1, col. 5-16).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iselt (US 6,917,582) in further view of Zhang (US 2003,016148).

In regard to claim 4, Iselt does not teach an information processing apparatus as claimed in claim 2, wherein said adjustment means further includes designation means for designating the frequency with which the discrimination is to be performed to a frequency lower than a frequency with which the output data of said first and second information processing means are received.

Zhang teach of a synchronous data serialization circuit where the application specific integrated circuit (ASIC) performs the monitoring and error correction functions at the lower frequency *(paragraph 0043)*.

It would have been obvious to modify the apparatus of Iselt by adding Zhang synchronous data serialization circuit. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would established telecommunication standards require the transceiver to perform various functions, including data monitoring and error correction *(paragraph 0043)*.

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3. Claims 21-24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iselt (US 6,917,582) in further view of Rey et al. (US 7036069).

In regard to claim 21, Iselt does not explicitly teach the information processing apparatus according to claim 20, wherein:

said error control means receives notifications of whether or not orders of said output data coincide with each other,

said error control means receives notifications of whether or not data values of said output data coincide with each other, and

said error control means receives notifications of whether or not an error of hardware failure exists.

Rey et al. teach the entity of packet loss distinction by implementing an error detection technique of bit error checking and a packet loss detection to distinguish packet losses during data transmission and to provide information on the kind of data loss. Also, Rey et al. teach of the main transport protocols used over IP networks are UDP and TCP to send acknowledgements to determine which packets have reached the receiver or identified the loss of a packet by the absence of an acknowledgement for the packet within a time out interval (*col. 1 lines 25-34).*

It would have been obvious to modify the apparatus of Iselt by adding Rey et al. entity of packet loss distinction. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would increase the network stability by controlling congestion in the network and increasing the transmission performance by compensating bit errors (*col. 2 lines 64-67).*

In regard to claim 22, Iselt teach the information processing apparatus according to claim 21 of said first or second information processing means (*ATM cell stream is split into two redundant data streams that are routed via different paths, fig. 1, col. 3 lines 5-10).*

Iselt does not explicitly teach the apparatus wherein said error of hardware failure may be a parity error, a protocol error, or timeout of a packet.

Rey et al. teach the entity of packet loss implementing a checksum (*col. 5 lines 17-26)* and time out interval (*col. 1 lines 30-34).*

Refer to claim 21 for motivational statement.

In regard to claim 23, Iselt teach the information processing apparatus according to claim 21, for said first and second information processing means (*ATM cell stream is split into two redundant data streams that are routed via different paths, fig. 1, col. 3 lines 5-10).*

Iselt does not explicitly teach the apparatus wherein in a case that said error control means receives a notification of incoincidence of said orders of said output data, or said error control means receives a notification of incoincidence of said data values of said output data, and said error control means does not receive a notification of an error of hardware failure, then said error control means executes a synchronism restoration process.

Rey et al. teach the entity of packet loss implementing error detection technique for determine if there were any errors during transmission via a checksum (*col. 5 lines 17-26)* and using a transport protocols over IP network wherein determination which

packet has reached the receiver by cumulative acknowledgements or the absence of an acknowledgement for the packet within a time out interval (*col. 1 lines 30-34).*

Refer to claim 21 for motivational statement.

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4. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iselt (US 6,917,582) in further view of Rey et al. (US 7036069) in further view of Galy et al. (US 5,689,632).

In regard to claim 24, Iselt and Rey et al. does not explicitly teach the information processing apparatus according to claim 21, wherein in a case that said error control means receives a notification of an error of hardware failure of one of said first or second information processing means, then said error control means performs a disconnection process of said one of said first and second information processing means.

Galey et al. teach the computing unit having a plurality of redundant computers wherein each microcontroller is equipped with a monitoring system known as a "guard dog" and when the microcontroller fails to refreshes it guard dog, the latter disconnects the power supply (*col. 4 lines 28-38).*

It would have been obvious to modify the apparatus of Iselt and Rey et al. by adding Galey et al. computing unit with plurality of redundant computers. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to

make the modification because it would able the system to operate without disturbance by the untimely starting operation of the other microcontroller (*col. 6 lines 25-30).*

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Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

- US 6,327,668 Williams

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LOAN TRUONG whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 9am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SCOTT BADERMAN can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
Art Unit: 2114

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER